COS 348C Schedule: Presenters and Papers

Tuesday, April 18

Pat Hanrahan: Rasterization Algorithms

- N. Gharachlorloo, S. Gupta, R. Sproull, I. Sutherland, A Characterization of Ten Rasterization Techniques, *Computer Graphics*, 23(3), 1989.

Thursday, April 20

Frank Crow: Parallel Rendering Algorithms

- F. Crow, Parallel Computing for Graphics.

Tuesday, April 25

Mike Marr: SLAM and Pixel Caching

- Demetrescu, High Speed Image Rasterization Using Scan Line Access Memories, Proceedings of the 1985 Chapel Hill Conference on VLSI, Computer Science Press.
- A. Goris, B. Frederickson, H. Baeverstad, A Configurable Pixel Cache for Fast Image Generation, *IEEE CG&A* 7(3), pp. 24-32, 1987.

Ziyad Hakura: Graphics Instruction Sets

- M. Tremblay, et. al. The Visual Instruction Set (VIS) in UltraSPARC, *Compcon Spring 95*, March 5-9 1995, San Francisco.
- J. Grimes, L. Kohn, R. Bharadhwaj, The Intel i860 64-bit Processor: A General-Purpose CPU with 3D Graphics Capabilities, *IEEE CG&A* 9(4), pp. 85-94, 1989.

Thursday, April 27

Michael Cox, Sun Microsystems

- S. Molnar, M. Cox, D. Ellsworth, H. Fuchs, A Sorting Classification for Parallel Rendering, *IEEE CG&A*, 14(4), pp. 23-31, 1994.

Tuesday, May 2

Kurt Akeley, Silicon Graphics Computer Systems

Thursday, May 4

Michael Deering, Sun Microsystems

- M. Deering, S. R. Nelson, Leo: A System for Cost Effective 3D graphics, *Computer Graphics*, pp. 101-108, 1993.
- M. Deering, S. Schlapp, M. Lavelle, FBRAM: A New Form of Memory Optimized for 3D Graphics, *Computer Graphics*, pp. 167-174, 1994.

Tuesday, May 9

Stephanie Winner, Apple

- M. Kelley, S. Winner, K. Gould, Scalable Hardware Render Accelerator Using A Modified Scanline Algorithm, *Computer Graphics* 26(2), pp. 241-248, 1992.

Thursday, May 11

Doug Voorhies, Silicon Graphics Computer Systems

Tuesday, May 16

Reid Gershbein: Low-latency Rendering

- M. Regan and R. Pose, Priority Rendering with a VR Address Recalculation Pipeline, *Computer Graphics*, pp. 155-162, 1994.
- G. Bishop, H. Fuchs, L. McMillan, E. Scher Zagier, Frameless Rendering: Double Buffering Considered Harmful, *Computer Graphics*, pp. 175-176, 1994.

Stuart Cheshire

- The GLINT Chip and other personal computer graphics chip-sets.

Thursday, May 18

Pierre St. Hiliare, Interval Research

Tuesday, May 23

Rob Engle: SGI GTX and RE

- K. Akeley, T. Jermoluk, High Performance Polygon Rendering, *Computer Graphics*, 22(4), pp. 239-246, 1988.
- K. Akeley, Reality Engine Graphics, *Computer Graphics*, pp. 109-116, 1993.

Jonathon Carter: Pixel Machine, GS1000

- B. Apgar, B. Bersack, A. Mammen, A Display System for the Stellar GS1000, *Computer Graphics*, 22(4), pp. 239-246, 1988.

- M. Potmesil and E. Hoffert, The Pixel Machine, *Computer Graphics*, 23(3), pp. 69-78, 1989.

Thursday, May 25

Maneesh Agrawala: Pixel Planes

- H. Fuchs, J. Poulton, Pixel-Planes: A VLSI-Oriented Design for a Raster Graphics Engine, *VLSI Design*, 2(3), pp. 20-28, 1981.
- H. Fuchs, J. Poulton, J. Eyles, T. Greer, J. Goldfeather, D. Ellsworth, S. Molar, G. Turk, B. Tebbs, L. Israel, Pixel Planes 5: A Heterogeneous Multiprocessor Graphics System Using Processor Enhanced Memories, *Computer Graphics*, 23(3), pp. 79-88. 1989.

Jeff Chan: Pixel Flow and Freedom 3000

- S. Molnar, J. Eyles, J. Poulton, PixelFlow: High-Speed Rendering Using Image Composition, *Computer Graphics*, 26(2), pp. 231-240, 1992.
- Freedom 3000
- Denali Technical Overview, Version 1.0, Kubota Pacific Computer, 1993.

Tuesday, May 30

Venkat Krishnamurthy: Parallel Rendering

- C. Mueller, The Sort-First Rendering Architecture for High-Performance Graphics, *Proc. 1995 Symposium on Interactive 3D Graphics*, pp. 75-84, 1995.
- S. Whitman, Dynamic Load Balancing for Parallel Polygon Rendering, *IEEE CG&A*, 14(4), pp. 41-48, 1994.

Homan Igehy: Parallel Rendering

- T. Crockett, T. Orloff, A Parallel Rendering Algorithm for MIMD Architectures, *Proc. Parallel Rendering Symposium*, ACM Press, NY, pp. 35-42, 1993.
- T. Crockett, T. Orloff, Parallel Polygon Rendering for Message-Passing Architectures, *IEEE Parallel and Distributed Technology*, 2(2), pp. 17-29, 1994.
- D. Ellsworth, A New Algorithm for Interactive Graphics on Multicomputers, *IEEE CG&A* 14(4), pp. 33-40, 1994.

Thursday, June 1

Andrew Beers: Shading

- M. Deering, S. Winner, B. Schediwy, C. Duffy, N. Hunt, The Triangle Processor and Normal Vector Shader: A VLSI System for High Performance Graphics, *Computer Graphics*, 22(4), pp. 21-30, 1988.
- A. Lastra, S. Molnar, M. Olano, Y. Wang, Real-time programmable shading, *Proc. 1995 Symposium on Interactive 3D Graphics*, pp. 59-66, 1995.